REMARKS

The Office Action mailed on October 22, 2002, has been received and reviewed. Claims 31-35 and 37-45 are currently pending in the above-referenced application. Each of claims 31-35 and 37-45 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 33, 34, 37-41, 44, and 45 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, it appears that each of claims 33, 34, 37-41, 44, and 45 has been rejected for reciting a structure which includes both hemispherical grain (HSG) polysilicon on or over a storage poly and dielectric material lining recesses that have been formed in the storage poly.

The argument that is presented in the outstanding Office Action are somewhat confusing:

> After a further review of the Specification, including the portion cited by Applicant, the Examiner agrees with Applicant that the Specification does not provide a written description of the presence of the layer HSG before the step of depositing a dielectric material 138. (Emphasis in original).

Office Action of October 22, 2002, pages 2 and 3. At no point during prosecution of the above-referenced application have Applicants stated or even hinted that the specification of the above-referenced application "does not provide a written description" of the presence of HSG polysilicon on a storage poly structure which has recesses formed therein that are lined with dielectric material. To the contrary, Applicants have pointed out that the specification does not provide a written description that the residual HSG polysilicon has been completely removed prior to lining recesses in the storage poly structure with dielectric material. Further, as the residual HSG polysilicon and the storage poly structure are both formed from polysilicon, it does not appear that there is any need to remove the remaining HSG polysilicon from the storage poly structure.

As for the assertion on page 3 of the outstanding Office Action that the specification and figures of the above-referenced application create an ambiguity, it is respectfully submitted that there is no ambiguity—either the HSG polysilicon remains or it does not. Nothing in the patent laws, rules, or M.P.E.P. precludes the inclusion of alternative embodiments in a patent application.

Moreover, the as-filed specification, at page 8, lines 20 and 21, quite clearly teaches that the mask layer material is removed, but does not mention removal of the remaining HSG polysilicon, making it unambiguous that the residual HSG polysilicon may remain on the structure depicted in FIG. 10.

Accordingly, withdrawal of the 35 U.S.C. § 112, first paragraph, rejections of claims 33, 34, 37-41, 44, and 45 is respectfully requested.

Rejections Under 35 U.S.C. § 102(b)

Woo

Claims 31-35 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,405,799 to Woo et al. (hereinafter "Woo").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Woo describes a structure that, as depicted in FIG. 2 thereof, includes a bottom conductive plate 16, conductive bars 23 thereon, and an upper conductive plate 25 over the bars 23, with the bars 23 electrically connecting the bottom conductive plate 16 and the upper conductive plate 25. At col. 4, lines 9-14, and in FIG. 10 Woo describes and illustrates the bars 23 as comprising polysilicon layers 18 that "remain as islands of various shapes" which are surrounded by remaining portions of a second insulating layer 17, which portions are also referred to in Woo as an insulating layer pattern 19.

Independent claim 31 recites a semiconductor storage capacitor poly that includes downwardly extending recesses and a plurality of contiguous mesas that comprise a plurality of contiguous top surfaces forming a maze-like structure.

Since Woo describes the polysilicon layers 18 as remaining "as *islands* of various shapes," (emphasis supplied) Woo cannot expressly or inherently describe that these structures comprise "a plurality of contiguous mesas" or that they form "a maze-like structure."

Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 31 is allowable over Woo.

Claim 32 is allowable, among other reasons, as depending from claim 31, which is allowable.

Independent claim 33 also recites a semiconductor capacitor storage poly. The capacitor storage poly of independent claim 33 includes downwardly extending recesses, a plurality of contiguous webs that comprise contiguous top surfaces, and hemispherical grain polysilicon on at least some of the contiguous top surfaces.

Woo neither expressly nor inherently describes a capacitor storage poly that includes a plurality of contiguous webs that comprise a plurality of contiguous top surfaces that form a maze-like structure. Instead of contiguous webs, the description of Woo is limited to polysilicon layers 18 which remain "as *islands* of various shapes." (Emphasis supplied).

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 33 is allowable over Woo.

Claim 34 is allowable, among other reasons, as depending from claim 33, which is allowable.

Independent claim 35, as amended and presented herein, recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a contiguous hemispherical grain polysilicon layer on and in contact with the storage poly structure, and a mask over the hemispherical grain polysilicon layer. Recesses in the storage poly structure are exposed through the contiguous hemispherical grain polysilicon layer and the mask.

As Woo describes that the polysilicon layers 18 depicted in FIG. 10 are *always* surrounded by remaining portions of a second insulating layer 17, Woo lacks any express or inherent description of an intermediate semiconductor capacitor structure that includes a storage capacitor poly with downwardly extending recesses.

In addition, Woo does not expressly or inherently describe a hemispherical grain polysilicon layer that is on and in contact with a storage poly structure. Rather, the description of Woo is limited to a polysilicon layer 18 that overlies and contacts an insulating layer 17 that is on a bottom conductive plate 16. *See* FIGs. 4 and 5; col. 3, lines 10-33.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(b), amended independent claim 35 is allowable over Woo.

Kenney

Claims 35 and 37-45 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,254,503 to Kenney (hereinafter "Kenney").

Kenney describes storage poly structures and methods for fabricating such structures. In particular, Kenney discloses two methods for forming high surface area storage poly structures, as well as two, corresponding intermediate structures. One structure, shown in FIG. 4 of Kenney, includes recesses 20 that are formed at areas that are located beneath regions where the high points of surface irregularities 14, such as hemispherical grain polysilicon, previously resided. It appears from FIG. 4 that the surface irregularities 14 may have been formed directly on the storage poly structure. The other intermediate structure, which is depicted in FIG. 5 of Kenney, includes surface irregularities 14, such as hemispherical grain polysilicon, which are formed on a layer 12 of silicon dioxide that, in turn, is formed over the storage poly structure. Col. 4, lines 50-55. Recesses 21 in the silicon dioxide layer 12 and, thus, in the storage poly structure are formed beneath locations where low-elevation regions of the surface irregularities 14 previously resided.

Independent claim 35, as amended and presented herein, recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a contiguous hemispherical grain polysilicon layer on and in contact with the storage poly structure, and a

mask over the hemispherical grain polysilicon layer. Recesses in the storage poly structure are exposed through the contiguous hemispherical grain polysilicon layer and the mask.

Kenney neither expressly or inherently describes that the structures shown in either FIG. 4 or FIG. 5 thereof includes a contiguous layer of hemispherical grain polysilicon. Instead, Kenney lacks any express or inherent description that both the surface irregularities 14 and the underlying region 12 of a substrate 10 may both be are formed from hemispherical grain polysilicon. Further, FIGs. 1-4 depict the surface irregularities 14, which may comprise hemispherical grain polysilicon, as being spaced apart from one another, not as being contiguous with one another.

The structure shown in FIG. 5 of Kenney does not include a contiguous layer of hemispherical grain polyslicon on and in contact with a storage poly structure *and* a mask over the hemispherical grain polysilicon layer. More specifically, Kenney lacks any express or inherent description that the structure shown in FIG. 5 thereof ever requires or includes a mask. Moreover, Kenney lacks any express or inherent description that the structure shown in FIG. 5 includes a contiguous layer of hemispherical grain polysilicon. Instead, if hemispherical grain polysilicon were used, lower-elevation regions thereof would have been removed to form recesses, with only the spaced-apart (*i.e.,* not contiguous), upper regions of the hemispherical grain polysilicon remaining. Further, the layer of hemispherical grain polysilicon shown in FIG. 5 is not in contact with the storage poly structure but, rather, with an intervening layer 12 of silicon dioxide. Col. 4, lines 50-55.

For these reasons, it is respectfully submitted that Kenney does not expressly or inherently describe an embodiment which anticipates each and every element of amended independent claim 35. Thus, under 35 U.S.C. § 102(b), amended independent claim 35 is allowable over Kenney.

Independent claim 37, as amended and presented herein, recites an intermediate semiconductor memory cell structure that includes a storage poly structure, a plurality of contiguous low elevation regions of a hemispherical grain polysilicon layer on and in contact with the storage poly structure, recesses formed in the storage poly structure laterally between the low elevation regions, and dielectric material at least lining the recesses.

In FIGs. 1-4 of Kenney, the low-elevation regions of the surface irregularities 14, which may or may not comprise hemispherical grain polysilicon, are shown as being spaced apart from one another, not as being contiguous with each other. As Kenney lacks any express or inherent description of a structure that includes a plurality of contiguous low elevation regions of a hemispherical grain polysilicon layer, it is respectfully submitted that Kenney does not anticipate each and every element of amended independent claim 37.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(b), amended independent claim 37 is allowable over Kenney.

Independent claim 38 recites a semiconductor memory cell structure that includes "regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure . . . and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses".

Kenney does not include any express or inherent description of a semiconductor memory cell structure that includes hemispherical-grain polysilicon on the top surfaces of a storage poly structure, the recesses of which are substantially coated with a dielectric layer. To the contrary, at col. 4, lines 38-40, Kenney provides for removal of the "mask forming layers" from at least the structure shown in FIG. 4, which "mask forming layers" appear to include both the surface irregularities 14 and the masking layer 16, prior to the formation of a dielectric coating within recesses of the resulting storage poly structure.

With respect to the description that accompanies FIG. 5 of Kenney, it is clear that if hemispherical grain polysilicon were used to form the surface irregularities 14, that the hemispherical grain polysilicon would not be located *on* a storage poly structure but, rather, on a layer 12 of silicon dioxide that, in turn, has been placed on the storage poly structure.

For these reasons, it is respectfully submitted that Kenney does not anticipate each and every element of independent claim 38 and, thus, that, under 35 U.S.C. § 102(b), independent claim 38 is allowable over Kenney.

Claims 39-41 are each allowable, among other reasons, as depending from claim 38, which is allowable.

Independent claim 42 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a substantially confluent hemispherical grain polysilicon layer on the storage poly structure, and a mask positioned over the hemispherical grain polysilicon layer. Elevated portions of the hemispherical grain polysilicon layer are exposed through the mask.

Kenney lacks any express or inherent description of an intermediate structure that includes a contiguous layer of hemispherical grain polysilicon. In particular, Kenney lacks any express or inherent description that both the surface irregularities 14 and the underlying region 12 of a substrate 10 may both be are formed from hemispherical grain polysilicon. Further, FIGs. 1-4 depict the surface irregularities 14, which may comprise hemispherical grain polysilicon, as being spaced apart from one another, not as being contiguous with one another.

Therefore, Kenney does not anticipate each and every element of independent claim 42. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 42 is allowable over Kenney.

Independent claim 43, as amended and presented herein, also recites an intermediate semiconductor capacitor structure. The intermediate semiconductor capacitor structure of amended independent claim 43 includes a storage poly structure with recesses therein, remaining portions of a hemispherical grain polysilicon layer substantially overlying upper portions of the storage poly structure, and a mask positioned over the hemispherical grain polysilicon layer. The mask is located laterally between the recesses in the storage poly structure, with the recesses being exposed therethrough, and is substantially spaced apart from the storage poly structure by way of the remaining portions of hemispherical grain polysilicon layer.

Kenney neither expressly nor inherently describes an intermediate semiconductor capacitor structure that includes portions of a hemispherical grain polysilicon layer that substantially overlie upper portions the storage poly structure or that the mask thereof is substantially spaced apart from storage poly structure by way of the remaining portions of the hemispherical grain polysilicon layer described therein. Instead, FIGs. 2-4 of Kenney, which are

the only figures in Kenney that illustrate a mask 16, quite clearly depicts the mask 16 as contacting the upper surface of item 12, which is apparently a storage poly structure.

Therefore, it is respectfully submitted that Kenney does not anticipate each and every element of amended independent claim 43 and, thus, that, under 35 U.S.C. § 102(b), amended independent claim 43 is allowable over Kenney.

Independent claim 44, as amended and presented herein, recites an intermediate semiconductor capacitor structure that includes a storage poly structure with recesses therein, a hemispherical grain polysilicon layer on at least portions of the storage poly structure, and dielectric material lining at least the recesses.

Again, Kenney lacks any express or inherent description of an intermediate semiconductor capacitor structure which includes both dielectric material lining the recesses that are formed in a storage poly structure and hemispherical grain polysilicon on portions of the storage poly structure.

Therefore, under 35 U.S.C. § 102(b), amended independent claim 44 is allowable over Kenney.

Independent claim 45, as amended and presented herein, is directed to an intermediate semiconductor memory cell structure that includes a storage poly with recesses therein, low elevation regions of a hemispherical grain polysilicon layer substantially covering an upper surface of the storage poly structure, and dielectric material at least lining the recesses.

Kenney neither expressly nor inherently describes an intermediate semiconductor capacitor structure which includes both dielectric material lining the recesses that are formed in a storage poly structure and hemispherical grain polysilicon that substantially covers an upper surface of the storage poly structure.

Accordingly, under 35 U.S.C. § 102(b), amended independent claim 45 is allowable over Kenney.

Ahn

Claim 42 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,358,888 to Ahn et al. (hereinafter "Ahn").

Ahn teaches a method for manufacturing a capacitor and the structures that result from that method. Among other things, Ahn teaches, at col. 6, lines 31-48, forming HSG polysilicon grains that are "slightly separated from one another, thereby being formed as a group of islands."

Independent claim 42 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a substantially confluent hemispherical grain polysilicon layer on the storage poly structure, and a mask positioned over the hemispherical grain polysilicon layer. Elevated portions of the hemispherical grain polysilicon layer are exposed through the mask.

As Ahn teaches that the hemispherical grain polysilicon layer thereof includes islands that are separated from one another, Ahn does not expressly or inherently describe a structure which includes a substantially confluent hemispherical grain polysilicon layer.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 42 is allowable over Ahn.

For the foregoing reasons, it is respectfully requested that the 35 U.S.C. § 102(b) rejections of claims 31-35 and 37-45 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 31-35 and 37-45 is allowable. An early notice of the allowability of each of these claims and an indication that the above-referenced application has been passed for issuance are respectfully solicited. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,

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Date: January 21, 2003

Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

35. (Thrice amended) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure comprising a plurality of contiguous mesas with recesses [formed therein] therebetween;

a contiguous hemispherical-grain polysilicon layer [over] on said storage poly structure and in contact therewith; and

a mask over said hemispherical-grain polysilicon layer, said recesses being exposed through said contiguous hemispherical-grain polysilicon layer and said mask.

37. (Twice amended) An intermediate semiconductor memory cell structure, comprising:

a storage poly structure;

a plurality of contiguous low elevation regions of a hemispherical-grain polysilicon layer on said storage poly structure;

recesses formed in said storage poly structure and located laterally between said plurality of contiguous low elevation regions of said hemispherical-grain polysilicon layer; and

dielectric material at least lining the recesses.

43. (Thrice amended) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure including recesses [formed] therein;

remaining portions of a hemispherical-grain polysilicon layer substantially overlying upper portions of said storage poly structure; and

a mask positioned over said hemispherical-grain polysilicon layer, laterally between said recesses, and substantially spaced apart from said storage poly structure by said remaining

portions of said hemispherical-grain polysilicon layer, said recesses in said storage poly structure being exposed through said mask.

44. (Amended four times) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure with recesses [formed] therein;

a hemispherical-grain polysilicon layer on at least portions of the storage poly structure; and

[a mask overlying at least portions of said hemispherical-grain polysilicon layer located laterally between said recesses; and]

dielectric material lining at least said recesses.

45. (Amended twice) An intermediate semiconductor memory cell structure, comprising:

a storage poly structure with recesses [formed] therein;

low elevation regions of a hemispherical-grain polysilicon layer on at least portions of the storage poly structure; and

[a mask overlying at least said low elevation regions of said hemispherical-grain polysilicon layer, said recesses being exposed between said low elevation regions of said hemispherical-grain polysilicon layer and through said mask; and]

dielectric material at least lining said recesses.